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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,577	ROY, RICHARD S.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,11-13 and 15-20* is/are rejected.

7)☒ Claim(s) *5-10 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handy "The Cache Memory Book" in view of Barroso et al. US Patent 6,675,265.

In regards to claim 1, Handy discloses a semiconductor memory circuit having a plurality of hierarchically organized levels, comprising:

a first level memory portion for storing data therein figure 2.23 L1 cache,

a second level memory portion for storing data therein figure 2.23 L2 cache, and

whereby data accessed from said second level memory portion is selectively loaded into said first level memory portion in a loading operation that is substantially simultaneous relative to accessing of said data in said second memory level portion figure 2.4 arrows on data bus feeding cache data memory and CPU simultaneously.

Handy does not disclose said first level memory portion having first level Data In (DIN) and Data Out (DOUT) buffer blocks associated therewith for effectuating data operations with respect to a location in said first level memory portion, said first level DIN buffer block including Local Data In (LDIN) driver circuitry;

said second level memory portion having second level Data In (DIN) and Data Out (DOUT) buffer blocks associated therewith for effectuating data operations with respect to a location in said second level memory portion;

or a multiplexing circuitry disposed in said first level DIN buffer block, said multiplexing circuitry being actuatable for providing data accessed through said second level DOUT buffer block to said LDIN driver circuitry in said first level DIN buffer block,

Barroso discloses an example of the input an output buffers in figure 10c element 408, Barroso also discloses a multiplexor for selectively feeding the contents of the data out buffer to the L1 cache via Mux element 416. It is well known in the art to use data in and data out buffers in conjunction with cache memory, especially in the case where the cache uses a single port memory, this is done to prevent the need for wait states when the cache in question is busy when a request is made. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate data input and output buffers with a cache memory and a multiplexor to feed data from L2 dato output buffer to the L1 data input buffer.

In regards to claim 2, Handy discloses in section 2.2.10 first two paragraphs how the design of a memory system comes down to a balancing of cost vs. performance and how DRAM is a the cheap solution and SRAM is the performance solution, therefore it would have been obvious to one of ordinary skill in the art at the time of invention to choose both L1 and L2 caches to consist of SRAM when one is choosing performance over cost.

In regards to claim 3, Handy discloses in section 2.2.10 first two paragraphs how the design of a memory system comes down to a balancing of cost vs. performance and how DRAM is a the cheap solution and SRAM is the performance solution, therefore it would have been obvious to one of ordinary skill in the art at the time of invention to choose first level memory portion comprises SRAM and the second level memory portion comprises dynamic RAM (DRAM) when trying to strike a balance between cost and performance.

In regards to claim 4, Handy discloses in section 2.2.10 the benefit in performance when using a tertiary cache therefore it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate a third level cache and organize the cache in a manner similar to the secondary cache. Additionally it would have been obvious to one of ordinary skill in the art at the time of invention to operate said third level cache in the same way as said first and said second memory levels.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Handy "The Cache Memory Book" in view of Shimpi "Intel Pentium III 1GHz".

Handy discloses in Figure 2.4b a semiconductor memory circuit having a plurality of hierarchically organized levels, comprising the steps of:

initiating a data access operation for accessing data in said semiconductor memory circuit (outward arrow from CPU on address line);

determining if said data is available in a first level memory portion of said semiconductor memory circuit (arrow entering cache-tag);

if not, accessing said data in a next level memory portion of said semiconductor memory circuit (arrow along address feeding through address buffer into main memory); and

selectively loading said data accessed from said next level memory portion into said first level memory portion in a loading operation that is substantially simultaneous relative to said accessing of said data in said next memory level portion (arrows on data bus feeding cache data memory and CPU simultaneously).

Handy does not disclose the next level of memory is integrated into the semiconductor memory circuit. Placing Handy's figure 2.4b within the context of figure 2.23, it is clear that the L2 cache takes the place of the main memory in figure 2.4b. In processing of a L1 cache miss and L2 cache hit, the L2 would be sourcing the simultaneous providing of data to the CPU and to the updating of L1 cache (the same as the main memory in figure 2.4b). Shimpi discloses that the Intel Pentium 3 under review on 8 March 2000, contains both an L1 and L2 that are both on die (3rd bullet of Specifications and page 2 6th paragraph). Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to integrate the next memory level into the semiconductor memory circuit for the purpose of increasing the systems performance.

Claims 12,13,15-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy "The Cache Memory Book" in view of Shimpi "Intel Pentium III 1GHz" in further view of common knowledge.

In regards to claim 12, Handy discloses in section 2.2.10 the benefit in performance when using a secondary cache therefore it would have been obvious to one of ordinary skill in the art at the time of invention to make the next level memory portion a second level memory portion of said semiconductor memory circuit.

In regards to claim 13, Handy discloses in section 2.2.10 the benefit in performance when using a tertiary cache therefore it would have been obvious to one of ordinary skill in the art at the time of invention to make the next level memory portion a third level memory portion of said semiconductor memory circuit.

In regards to claim 15, Handy discloses that the data presented on the data bus is dependent upon the address on the address bus and in the event of an L1 cache miss, data fed from L2 to L1 is simultaneously loaded into L1 and the CPU when the address is presented to the L2 cache.

In regards to claim 16, Handy discloses in section 2.2.10 first two paragraphs how the design of a memory system comes down to a balancing of cost vs. performance and how DRAM is a the cheap solution and SRAM is the performance

solution, therefore it would have been obvious to one of ordinary skill in the art at the time of invention to make the first level memory portion of static random access memory (SRAM) when choosing performance over cost.

In regards to claim 17, Handy discloses in section 2.2.10 first two paragraphs how the design of a memory system comes down to a balancing of cost vs. performance and how DRAM is a the cheap solution and SRAM is the performance solution, therefore it would have been obvious to one of ordinary skill in the art at the time of invention to make the first level memory portion from dynamic RAM (DRAM) when choosing cost over performance.

In regards to claim 18, Handy discloses in section 2.2.10 first two paragraphs how the design of a memory system comes down to a balancing of cost vs. performance and how DRAM is a the cheap solution and SRAM is the performance solution, therefore it would have been obvious to one of ordinary skill in the art at the time of invention to make the next level memory portion of static random access memory (SRAM) when choosing performance over cost.

In regards to claim 19, Handy discloses in section 2.2.10 first two paragraphs how the design of a memory system comes down to a balancing of cost vs. performance and how DRAM is a the cheap solution and SRAM is the performance solution, therefore it would have been obvious to one of ordinary skill in the art at the

time of invention to make the next level memory portion from dynamic RAM (DRAM) when choosing cost over performance.

In regards to claim 20, Handy discloses in section 2.2.10 first two paragraphs how the design of a memory system comes down to a balancing of cost vs. performance and how DRAM is a the cheap solution and SRAM is the performance solution, therefore it would have been obvious to one of ordinary skill in the art at the time of invention to make the first and second level memory portions from SRAM or DRAM.

Allowable Subject Matter

Claims 5-10 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 13 May 2001 have been fully considered but they are not persuasive.

Applicant states that Handy fails to disclose the next level memory portion is integrated within the semiconductor memory circuit. Examiner has supplied Shimpi, "Intel Pentium III 1Ghz" to show that the incorporation of L2 cache (next level memory) on the processor die (6th paragraph of 2nd page) was well known in the art at the time of

invention. This renders applicant's claim limitation of an integrated next level memory as obvious to one of ordinary skill in the art at the time of invention.

As per applicant's assertion that Handy does not teach selective loading of data accessed from the next level memory into the first level memory portion in a loading operation that is substantially simultaneous relative to the accessing of the data in the next memory level portion (emphasis added by applicant). Examiner asserts that Handy selects to update the first memory level whenever this is a cache miss of that level. Examiner additionally asserts that Handy discloses as previously stated that the L1 cache (first memory level) updates its contents after a cache miss with data presented to the CPU by the next level memory as is shown in figure 2.4b. The loading operation *must* occur at the same time as the data is being presented for the correct data to be loaded into the cache. This operation cannot occur in any other fashion in Handy's disclosed system since the L1 cache is incapable of generating memory requests itself (as evidenced by no outward arrows from the cache memory elements onto the address bus) and must update its contents during a CPU request to a next memory level. Therefore, the cache controller performs a load operation that is simultaneous to the CPU's accessing of data in the next level memory portion.

For these reasons the examiner respectfully maintains his rejection of applicant's amended claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703)306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 7/26/04

PB

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER